Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.013”**

**.013”**

**ANODE**

**.006 x .006”**

\***DO NOT BOND TO CENTER AREA\***

**Top Material: AlSi**

**Backside Material: AuSb**

**Bond Pad Size: .006” X .006”**

**Backside Potential: Cathode**

**Mask Ref: BZX55**

**APPROVED BY: DK DIE SIZE .013” X .013” DATE: 7/13/22**

**MFG: VISHAY THICKNESS: .007” P/N:BZX55C10**

**DG 10.1.2**

#### Rev B, 7/19/02